

# Production of the Detector Assemblies for the Lunar Electromagnetic Monitor in X-rays

## *Statement of Work*

### Context

The goal of this contract is the manufacturing and integration of the Detector Assemblies (DAs) for the Lunar Electromagnetic Monitor in X-rays (LEM-X). Each DA is composed of a Front-End Board (FEB) populated with passive and active components and integrated with 24 Application Specific Integrated Circuits Front-End (ASICs FE), a Silicon Drift Detector (SDD), a flex-rigid PCB, wrap-around and a custom thermo-mechanical structure. The Front-End Board will represent the single mechanical, thermal and electrical interface between the Silicon Drift Detector and the LEM-X instrument. The DAs to be produced in this contract will exploit the heritage of the front-end electronics for the WFM aboard the eXTP satellite mission.

LEM-X is planned to operate on the Lunar surface, thus shall be designed to withstand the thermo-mechanical stresses at launch and the harsh environment on the Moon, in terms of radiation damage, temperature, dust and meteoroids, for a minimum lifetime of five years.

The detector is glued to the FEB with thin adhesive spots for mechanical and thermal connection. Detector and FEB together are called the "sandwich". The "sandwich" has strict requirements for alignment stability in all directions over the operational temperature range. Bending of the "sandwich" due to differences in coefficient of thermal expansion (CTE) shall be within these limits. Integrity of the adhesive spots shall not deteriorate over lifetime by stress due to CTE differences over the full applicable temperature ranges.

The technology for the FEB shall fulfil the alignment requirements over the whole temperature range (see section "Requirements"). For this reason, suitable materials for the FEB substrate are Al<sub>2</sub>O<sub>3</sub> or AlN with thick-film technology, exploiting the eXTP/WFM heritage. IAPS will perform a thermo-elastic analysis of the FEB model to verify the compliance with the requirements. The contractor has the task to perform a thermo-mechanical test of the same FEB, based on the input from the analysis by IAPS.

The FEB shall include two rows of 12 naked ASICs FE dies, adjacent to each other, each row on opposite edges of the board. Each ASIC has, on one side, 32 input channels, with a pitch of 150 µm, that are wire bonded directly to the detector, whose anode pitch is 169 µm. The other side of the ASIC has 44 (TBC) pads with wire bonds to the FEB, with a pitch of 103.4 (TBC) µm. The FEB will have an electrical interface with the supplying Back-End Electronics unit (BEE) via two coaxial high-voltage cables and a flex-rigid PCB.

The required trace density and number of signal layers is determined by

- (1) the fine pitch of I/O pads on the ASICs FE,
- (2) the high amount of connections needed between the ASICs FE and the FEB and
- (3) the high amount of connections needed between the FEB and the Back-End Electronics unit.

Furthermore, a number of passive parts and potentially a foil heater shall be placed on the FEB. A limited part of the printed circuit shall conduct high voltages, up to -1300 V (-2600 V after including a safety margin), to be filtered and fed to the detector via wire bonds.

## Requirements

The following requirements are applicable to the printed circuit board of the FEB. Most numbers given are not final but good estimates. The final values will be provided by the customer at the Kick-off meeting of the contract

- **Dimensions approximately 70 x 65 mm<sup>2</sup> (TBC), nominal thickness 1.5 mm (TBC). Specific shape and geometry required**
- **The FEB lateral dimension tolerance shall be  $\pm 0.1$  mm**
- **The FEB thickness tolerance shall be  $\pm 0.15$  mm**
- **Baseline material shall be Al<sub>2</sub>O<sub>3</sub> ceramic (96 %) with thick-film technology**
- **Trace density (pitch)  $\geq 100$   $\mu$ m**
- **Thermal conductivity of substrate  $> 24$  W/(m·K)**
- **CTE of substrate**
  - $\leq 5$   $\mu$ m/(m · K) for T from -65 °C to +20 °C
  - $\leq 7.2$   $\mu$ m/(m · K) for T from +20 °C to +75 °C
- **Temperature range**
  - **operational: from -65 °C to +30 °C TBC**
  - **non-operational: from -70 °C to +80 °C TBC**
- **Glue selected in order to guarantee the connections over lifetime (five years) and over non-operational temperature range**
- **Compliant with high voltages up to 2600 V for a limited area of the PCB**
- **No potting or other encapsulation allowed for any naked die or wire bonding**
- **The FEB and all its components shall be designed to withstand a total radiation dose of 100 krad**

The electrical layout of the FEB will be provided by the Customer as input in KiCAD EDA (TBC) format and, if needed, shall be fine-tuned by the Contractor in open collaboration with the Customer, according to design rules compliant with the thick-film technology. The possibility of re-work of ASICs is a must. Customer and Contractor will jointly evaluate the re-work procedure and will study the possibility to mount replacement ASICs on-top of faulty ASICs.

## Summary of contractor tasks

- General list
  - Front-end board (FEB) thick film design, material sourcing and realisation
  - Wrap around boards design, material sourcing and realization
  - Surface Mount assembly of FEBs and wrap arounds including material sourcing
  - ASIC die- and wirebonding
  - HV/MV cable sourcing, connector attachment and soldering to FEB
  - Assembly/production tooling design & realization
  - Transport packaging design and realization
  - Documentation
- Front-End Board production
  - Adaptation of the electronic layout to the thick-film technology
  - FEB manufacturing on thick film substrate (printed circuit board, additional tabs and wrap-around) made of Al<sub>2</sub>O<sub>3</sub> or AlN or other suitable materials approved by IAPS

- Procurement of all materials and components, except ASICs. SMT components to be selected are of AEC-Q200 and/or MIL grade (TBC) with the same footprint and value of components in the ESA preferred part list
- Surface mount assembly/reflow on FEB and WA's
- Flux residue removal by waterfree cosolvent cleaning (vapor phase)
- Flying probe validation testing of printed circuitry
- Dicing: depaneling and making incision for later test connector removal
- Assembly of connector on FEB (for connecting to flex)
- Assembly of HV/MV connector cable and attachment to FEB by soldering
- Die- and wirebonding of ASICs on FEB
- Mechanical samples
  - Manufacturing of FEBs, without components but including test connector and diced incision that will be used by IAPS for all types of mechanical assembly testing
  - Wrap arounds without components for mechanical assembly testing
- Tooling
  - All production tooling for FEB assembly including printing screens, solder stencils, plotfilms, carriers, pickup tooling, wirebonding tooling, wirebonding toolplate.
  - Design and realization of 6 pcs transport packages for FEB's with bonded ASICs and having removable test part
- Testing
  - flying-probe testing of FEB interconnection boards

## List of Contractor deliverables

- 6 (TBC) Front-End Boards equipped with passive and active components, and ASICs (**DEL 1 – 6**)
- 6 Bare Front-End Boards, i.e. with no components assembled plus 6 sets wrap arounds mechanical samples, without components (**DEL 7**)
- 6 shipping containers for the 6 FEBs (**DEL 8**)
- Documentation
  - Integration flow document (**DEL 13**)
  - FEB Design Report (**DEL 9**)
  - Declared Materials List (**DEL 10**)
  - Declared Components List (**DEL 11**)
  - Declared Process List (**DEL 12**)

Special care during handling and environment considerations:

- ASIC inputs at the edges are extremely ESD sensitive. All handling shall be performed in agreement with a customer approved ESD control procedure
- Naked wire bonds at the edges are extremely vulnerable; sufficient measures shall be taken and tooling manufactured
- All activities and storage shall be carried out in clean room environment
- Interaction between contractor and customer during assembly and test activities shall be facilitated.

The design shall be according to ECSS design rules. All materials shall be vacuum compatible, with low outgassing (TML < 1 %, CVM < 0.1 %). All processes used for manufacturing and assembly shall be in line with ECSS standards. Components to be selected are of AEC-Q200 and/or MIL grade (TBC) with the same footprint and value of components in the ESA preferred part list.

No export control limitations are expected for parts, materials and processes.

The overall activity is requested to have a nominal maximum duration of 9 TBC months. This duration may be extended without cost variation if the duration of the LEM-X project is extended.

### Customer (IAPS) Furnished Items

- Electronic design, layout and Mechanical design of Front-End Boards
- Bill of Materials for Front-End Boards
- ASICs FE to be integrated on FEBs

### Notional schedule for the contract

- Kick-off Meeting: around May – June 2024
- FEB design review: 22/7/2024
- Delivery from IAPS of electronic design, layout, mechanical design and BOM: 22/7/2024
- Shipment of 6 Bare Front-End Boards to IAPS: 18/11/24
- Need date of FEB with components: 18/11/24
- Need date of ASICs at Contractor: 18/11/24
- Start of assembly of FEBs with ASICs: 18/11/2024
- FEB Delivery Review and shipment to IAPS: 20/01/25

Periodic progress meetings with frequency about twice per month will be planned between Customer and Contractor.

### Milestones / Gates and payments

Event	Date	Payment	Deliverables
Kick-off	T0		
Gate 1	T0 + 2 months	10 %	<ul style="list-style-type: none"> <li>• DEL 13</li> </ul>
Gate 2	T0 + 6 months	30 %	<ul style="list-style-type: none"> <li>• DEL 7</li> <li>• DEL 9</li> </ul>
Gate 3	T0 + 9 months	60 %	<ul style="list-style-type: none"> <li>• DEL 1 – 6</li> <li>• DEL 8</li> <li>• DEL 10</li> <li>• DEL 11</li> <li>• DEL 12</li> <li>• DEL 14</li> <li>• DEL 15</li> </ul>

### Risk table and mitigation

The Severity and Likelihood of each risk are defined following the document ECSS-M-ST-80C (31 July 2008).

Likelihood	Risk Index: Combination of Severity and Likelihood				
	1	2	3	4	5
E	Low	Medium	High	Very High	Very High
D	Low	Low	Medium	High	Very High
C	Very Low	Low	Low	Medium	High
B	Very Low	Very Low	Low	Low	Medium
A	Very Low	Very Low	Very Low	Very Low	Low

Severity

"Red"
  "Yellow"
  "Green"

Figure 5-5: Example of risk index and magnitude scheme

Risk index	Risk magnitude	Proposed actions
E4, E5, D5	Very High risk	Unacceptable risk: implement new team process or change baseline – seek project management attention at appropriate high management level as defined in the risk management plan.
E3, D4, C5	High risk	Unacceptable risk: see above.
E2, D3, C4, B5	Medium risk	Unacceptable risk: aggressively manage, consider alternative team process or baseline – seek attention at appropriate management level as defined in the risk management plan.
E1, D1, D2, C2, C3, B3, B4, A5	Low risk	Acceptable risk: control, monitor – seek responsible work package management attention.
C1, B1, A1, B2, A2, A3, A4	Very Low risk	Acceptable risk: see above.

Figure 5-6: Example of risk magnitude designations and proposed actions for individual risks

Figure 1: Risk classification from ECSS-M-ST-80C (31 July 2008)

### Risk table

Description	Severity	Likelihood	Risk Index
Delay in the production/delivery of ASICs FE	3	C	Low